## REMARKS

The Examiner is thanked for the thorough examination of the present application and the continued indication that claims 7-14 define allowable subject matter. The Office Action, however, continued to reject the remaining claims 1-6 and 15-20. Specifically, claims 1-5, and 15-20 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by *Olarig* U.S. Patent 6,038,680. Claim 6 stands rejected under 35 U.S.C. §103(a) as allegedly unpatentable in view of *Olarig* over *Ohran* Patent Application Publication 2002/0099916.

The present Office Action sets for the same substantive rejections that were set forth in the previous Office Action. Therefore, Applicant continues to traverse these rejections for the same reasons advanced in Applicant's previous response (thereby preserving these arguments for appeal). In addition, Applicant sets forth the following additional remarks, which respond to the "Response to Applicant's Argument" section of the FINAL Office Action (beginning on p. 6).

In page 8, the Office Action states:

> "…that module 55b is ready to carry the request addressed to module 55a from the point where the failure happened . In order to accomplish that, module 55b must have all the information that was requested before the failure, **in other words all the requests sent to module 55a must be sent to module 55b, and the only way to do that is by sending write requests to both module 55a and 55b**. From the above demonstration, it is clear that Oralig does not only write to module 55a, but also writes to module 55b in contrary to Applicant's argument."

(*Emphasis added*)

It appears that the point Applicant was trying to make was not fully expressed or not clearly understood. In this regard, Applicant's claims specify that the data is written

to the memory modules in a single write cycle. For example, independent claim 1 specifies: "wherein each of the memory mirror units writes data to the corresponding memory modules during a write cycle." Likewise, independent claim 15 specifies: "writing data to the corresponding memory modules according to a write address during a write cycle." Similarly, independent claim 18 specifies: "writing data to first and second memory modules according to a write address during a write cycle." That is, each of the independent claims specifies writing data to the plurality of memory moduleS during A write CYCLE (emphasis added). The express claim language is clear and unambiguous, and the only proper way to interpret it is that data is written into a plurality of memory modules during a single write cycle. It cannot be properly interpreted as writing data into a plurality of memory modules, with each module being written in a write cycle (such a construction reads in features that are not claimed, and ignores language that is expressly recited. This appears, however, to be the interpretation presently accorded to the claims.

In contrast to the claimed features, *Olarig* stores the same information in modules 55a and 55b during two write cycles. This operating principle of *Olarig* is described in the following. Col. 7, lines 6-13 of *Olarig,* which states:

> "When a predetermined fault condition, such as those discussed above is detected, the memory address controller 29 operates the hot swap logic 76. The logic 76 then checks to determine whether a module is present in a connector 57. **If so, the logic 76 signals the controller 29 to read the information from the problem module and to write the information into a module connected to the auxiliary connector 57**."

(*Emphasis added*)

*Olarig* writes information into module 55a during a write cycle. When a predetermined fault condition occurs, a controller reads the information from module

55a during a read cycle and writes the read information into a module 55b during another write cycle. Since *Olarig* does not simultaneously write information into modules 55a and 55b during only one write cycle, the information stored in module 55a must be read and then the read information is written into module 55b such that module 55b can substitute for module 55a. Thus, *Olarig* requires two write cycles to make the information stored in modules 55a and 55b the same.

Independent, the claim 1 is as below.

> 1. A computer system, unaffected by memory module instability, comprising:
> at least one memory mirror unit controlling a plurality of memory modules and receiving an error control signal, wherein **each of the memory mirror units writes data to the corresponding memory modules during a write cycle** and activates a first memory module among the memory modules, reading data during a read cycle;
> a memory controller enabling the error control signal upon detection of a read error in the first memory module, wherein the memory mirror unit disables the first memory module and activates a second memory module among the memory modules when the read error occurs in the first memory module.

(*Emphasis added*)

As noted above, and in comparison with *Olarig*, the application stores the same data into memory modules during only one write cycle. Since *Olarig* does not disclose how to utilize a write cycle to store the same information in modules and the limitation, that writes data to memory modules during one write cycle, occurs in independent claims 1, 15, and 18 of the application such that *Olarig* does not discloses all the limitations expressly recited in independent claims 1, 15, and 18 of the application. For at least this reason, the rejections should be withdrawn.

Response To Claim Rejections Under 35 U.S.C. §102(b)

Claims 1-5, and 15-20 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by *Olarig* U.S. Patent 6,038,680. However, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). *Olarig* does not disclose all limitations in the claims 1, 15, and 18 and the rejections should be withdrawn.

Independent, the claim 1 recites:

> 1. A computer system, unaffected by memory module instability, comprising:
> at least one memory mirror unit controlling a plurality of memory modules and receiving an error control signal, wherein **each of the memory mirror units writes data to the corresponding memory modules during a write cycle** and activates a first memory module among the memory modules, reading data during a read cycle;
> a memory controller enabling the error control signal upon detection of a read error in the first memory module, wherein the memory mirror unit disables the first memory module and activates a second memory module among the memory modules when the read error occurs in the first memory module.

(*Emphasis added*)

Independent, the claim 15 recites:

> 15. A method for controlling memory of a computer system, the method comprising the steps of:
> providing at least one memory mirror unit, each controlling a memory module group having a plurality of memory modules;
> equalizing addresses of the memory modules inside each memory module group;
> **writing data to the corresponding memory modules according to a write address during a write cycle**; and
> reading a first memory module according to a read address during a read cycle;

wherein the computer system activates an error control signal received by the corresponding memory mirror unit to select a second memory module from corresponding memory modules when a read error occurs in the first memory module.

(*Emphasis added*)

Independent, the claim 18 recites:

18. A method for controlling memory of a computer system, the method comprising the steps of:
providing at least one the memory mirror unit each controlling a first and second memory module;
equalizing addresses of the first and second memory modules;
**writing data to first and second memory modules according to a write address during a write cycle**; and
reading the corresponding first memory module according to a read address reading data during a read cycle;
wherein the computer system activates an error control signal received by the corresponding memory mirror unit to select a corresponding second memory module when a read error in the corresponding first memory module is detected.

(*Emphasis added*)

Taking one memory mirror unit as an example, if the memory mirror unit of the claimed embodiments controls a plurality of memory modules, when the error control signal is deactivated, the memory mirror unit of the invention writes data to the plurality of memory modules during the write cycle.

Col. 5, lines 59-67 of *Olarig* states:

"The hot swap logic 76 includes a threshold register to accumulate the number of errors which occur at particular locations as reported by the ECC logic 79. The threshold register, in concert with the memory interface 72. may undertake a comparison of the number of errors that occur with a predetermined fault threshold. When the comparison indicates that the predetermined threshold has been exceeded, a signal is transmitted to the hot swap logic 76 to implement corrective action"

Further, col. 6, line 64 - col 7 line 13 of *Olarig* states:

> "The hot swapping of modules may be accomplished in a variety of circumstances. For example, when threshold information in the register 68 indicates that a predetermined number of errors have occurred, the responsible module may be replaced. Ideally, the module may be replaced before a catastrophic failure causes system shut down. Alternatively, on the detection of an uncorrectable error, a hot swap operation may be initiated.
>
> When a predetermined fault condition, such as those discussed above is detected, the memory address controller 29 operates the hot swap logic 76. The logic 76 then checks to determine whether a module is present in a connector 57. If so, **the logic 76 signals the controller 29 to read the information from the problem module and to write the information into a module connected to the auxiliary connector 57**."

(*Emphasis added*)

Clearly, *Olarig* writes information into one module 55a during a write cycle. When threshold information in the register 68 indicates that a predetermined number of errors have occurred, *Olarig* reads the information from the problem module and to write the information into an auxiliary module 55b and writes information into the auxiliary module 55b. Thus, *Olarig* does not write information into the auxiliary module 55b during the write cycle when the number of errors does not arrive to a preset value.

Since *Olarig*, at least, does not disclose all of the defining limitations of independent claims 1, 15, and 18 (that each of the memory mirror units writes data to the corresponding memory modules during a write cycle), the rejections of claims 1, 15, and 18 under 35 U.S.C 102(b) should be withdrawn.

Consequently, *Olarig* does not disclose, suggest or teach all the features recited by claims 1, 15, and 18 of the present invention, and the rejections are respectfully traversed. Insofar as claims 2-5 depend from claim 1, claims 16-17 depend from claim 15, and claims 19-20 depend from claim 18, the 102 rejections of claims 2-5, 16-17, and 19-20 should be withdrawn as well.

Response To Claim Rejections Under 35 U.S.C. §103(a)

Claim 6 is rejected under 35 U.S.C. §103(a) as allegedly unpatentable in view of *Olarig* over *Ohran* Patent Application Publication 2002/0099916. *Olarig* and *Ohran*, individually or collectively, fail to disclose all the claim limitations in the claimed invention, however. To establish *prima facie* obviousness of a claimed embodiments, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

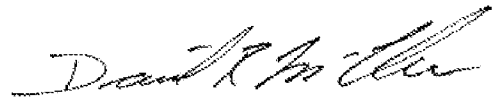
As discussed in connection with the patentability of the independent claim 1, *Olarig* fails to that all memory modules are written data during a write cycle. The same claimed feature lacked in *Olarig* can be found nowhere in *Ohran*. Consequently, since *Olarig* and *Ohran* do not disclose, suggest or teach all the features recited by claim 1 of the present application, *Olarig* and *Ohran* cannot render claim 1 anticipated or obvious, and claim 1 should be allowable over the references of record. Since claim 6 depends to allowable claim 1 to incorporate all the claimed features in claim 1, they, as a matter of law, should be allowable.

## ***CONCLUSION***

In light of the foregoing and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-20 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested.

If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

By: 

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